Section III. REMARKS

Acknowledgement of Examiner's Withdrawal of Claims 25-49 and Intention to Rejoin

The withdrawal of claims 25-49 as a result of restriction requirement is hereby acknowledged.

In the March 14, 2003 Office Action, a restriction requirement was imposed against the following claim groups:

I. Claims 1-24 and 50, drawn to a wafer susceptor; and

II. Claims 25-49, drawn to a method of increasing the throughput of a single substrate deposition chamber.

Applicant hereby confirms the provisional election of Group I claims 1-24 and 50 made by William Ryann, Esq. on February 19, 2003.

Applicants hereby express the intention to rejoin the non-elected Group II method claims 25-49 at a later time, or alternatively, with reservation of the right to file divisional application(s) directed to the subject matter of those claims if rejoinder is not effected.

In light of the fact that the elected Group I claims 1-24 and 50 relate to a product (i.e., a wafer holder) and the non-elected Group II claims 25-49 relate to the method of using such product, and that the non-elected Group II method claims include all the limitations of the elected product claim 1, Applicant intend to rejoin the non-elected Group II method claims 25-49 when the elected Group I product claims 1-24 and 50 are determined to be allowable.

The basis for such rejoinder is provided by MPEP §821.04, which states that when the application as originally filed discloses a product and the process for making and/or using such product, and only claims directed to the product are presented for examination, when a product claim is found allowable, applicant may present claims directed to the process of making and/or using the patentable product for examination through rejoinder procedure, provided that the process claims depend from or include all the limitations of the allowed product claims.

Consistent with such provisions of MPEP §821.04, if the product claim 1-24 and 50 are subsequently found allowable, the withdrawn method claims 25-49 will be properly rejoined for examination.

Therefore, Applicants will request the Examiner to take up the non-elected method claims 29-49 for examination when product claims 1-24 and 50 are allowed, and such non-elected method claims are thus amended herein, consistent with the amendments of the product claims 1-24 and 50, to prepare such non-elected method claims 25-49 for future examination once the rejoinder is granted.

Alternatively, if the rejoinder of the non-elected method claims 25-49 is denied, despite the proper basis in the MPEP therefor, applicants hereby reserve the right to file divisional application(s) directed to the subject matter of such withdrawn method claims under 35 U.S.C. 121.

Objections of Claims 4-24 and 50

The Examiner's objections to claims 4-24 and 50 in the March 14, 2003 Office Action for improper dependency have been overcome by amendments of claims 4-24 and 50 herein.

§112 Rejections of Claims 1-24 and 50

The Examiner's rejections of claims 1-24 and 50 under 35 U.S.C. §112, second paragraph, for lack of antecedent basis and/or for improper dependency, have been overcome by amendments of claims 1-24 and 50 herein.

§102(e) Rejection of Claims on the Basis of Suda et al.

In the March 14, 2003 Office Action, the Examiner rejected claims 1-3 under 35 U.S.C. §102(e) as being anticipated by **Suda** et al. U.S. Patent No. 6,053,980 (hereinafter "Suda").

In response, independent claim 1 (from which claims 2-24 depend) and claim 50 have been amended.

Applicant hereby traverses the Examiner's claim rejections, for the following reasons:

Claim 1, from which claims 2-24 depend, has been amended to recite:

> "A wafer susceptor for use in a substrate processing system, comprising:
>
> at least one recess formed therein, wherein each recess is arranged and configured to hold one substrate therein, **wherein said at least one substrate comprises material selected from the group consisting of silicon, gallium nitride, and aluminum nitride, and wherein said water susceptor is characterized by physical properties that match those of the substrates held therein**."

Claim 50 has been amended to recite:

> "A wafer susceptor used in a semiconductor substrate processing system, comprising at least one recess formed therein, wherein each recess is arranged and configured to hold one semiconductor substrate therein, **wherein said at least one semiconductor substrate comprises material selected from the group consisting of silicon, gallium nitride, aluminum nitride, diamond, gallium arsenide, indium nitride, indium phosphide, and gallium phosphide, wherein said wafer susceptor is characterized by physical properties that match those of the semiconductor substrates held therein**."

An important aspect of the present invention relates to the **provision of a wafer susceptor that has physical properties that match those of the substrates to be held thereby**. In such manner, the wafer substrates and the wafer susceptor "display **uniform material and physical properties** during the wafer processing" (see the instant specification, page 10, lines 6-8, which specifically states that wafers previously processed in batch tools do not display uniform physical properties such as thermal conductivity with the wafer susceptor), and **the wafer susceptor and the wafer substrates held thereby act as a composite substrate** for the purpose of processing, **as opposed to prior art wafer susceptor that merely functions as a support structure** for holding and/or supporting the wafers during batch processing (see the instant specification, page 9, lines 16-20).

The Suda reference cited by the Examiner only discloses a heat-resistant substrate holding means, which can be "made of quartz, glass, ceramics or metal," and which is preferably made of ceramics such as "a sintered SiC, a sintered SiC on which SiO_2 film is CVD-coated, and an alumina and the like" (see Suda, column 23, lines 15-35).

Suda, unlike the present application, does not appreciate the advantages of using a wafer holder that has physical properties that match with those of the substrate to be processed. Nor does Suda require use of such wafer holder with matching physical properties, as the claimed invention of the present application does.

Instead, the only quality Suda requires for its substrate holder is heat resistance, and such heat resistant materials listed by Suda are mostly non-semiconductor materials (quartz, glass, and alumina are all insulating materials, and metals are conducting materials), except for sintered SiC, which happens to be a semiconductor. Such non-semiconductor materials disclosed by Suda (i.e., quartz, glass, alumina, and metal) have physical properties that do not match with those of the semiconductor substrates to be processed. More specifically, the thermal conductivity, the electrical resistivity, the dielectric constant, and the dielectric loss of such insulating or conducting materials are significantly different from those of the semiconductor substrates.

On page 14 of the instant specification, it is disclosed that the "substrates may be formed from Silicon, GaN, SiC, AlN or other such material that is commonly used in the semiconductor industry."

On the basis of such disclosure, claims 1-24 and 50 of the present application have been herein amended to require substrates made of known semiconductor materials, such as silicon, GaN, AlN, diamond, GaAs, InN, InP, and/or GaP, specifically excluding SiC. The wafer holder as claimed by claims 1-24 and 50 therefore has to be made of materials having matching physical properties with those of such known semiconductor materials other than SiC.

None of the materials disclosed by Suda, i.e., quartz, glass, sintered SiC, alumina, and metal, has matching physical properties with substrates made of silicon, GaN, AlN, diamond, GaAs, InN, InP, and/or GaP, as required in claims 1-24 and 50.

Moreover, **Suda does not provide any derivative basis for using materials that have matching physical properties with substrates made of silicon, GaN, AlN, diamond, GaAs, InN, InP, and/or GaP in forming the wafer holder**.

Since a merely heat resistant material such as quartz, glass, sintered SiC, alumina, or metal is sufficient for providing the heat resistance required by the substrate holder disclosed by Suda, a person ordinarily skilled in the art, after reading Suda, would not have been motivated to modify such substrate holder by using a different material, much less to form a substrate holder with a material of matching physical properties with those of the substrates comprising silicon, GaN, AlN, diamond, GaAs, InN, InP, and/or GaP, as required by claims 1-24 and 50 of the present application.

Therefore, claims 1-24 and 50 patentably distinguish over the teachings in Suda, and the Examiner is hereby requested to reconsider, and upon consideration to withdraw, the rejections of such claims.

Withdrawn claims 25-49 have been hereby amended to recite corresponding limitations as in claims 1-24, and they therefore also patentably distinguish over the teachings in Suda, for the above-stated reasons.

New Claims 51 and 52

Newly added claim 51, from which claim 52 depends, recites:

> "A wafer susceptor arranged and configured **for placement in a single substrate deposition chamber**, wherein said wafer susceptor is **substantially circular in shape** and **comprises two or more recesses formed therein**, wherein each recess is arranged and configured to hold one substrate, and wherein said water susceptor is characterized by physical properties that match those of the substrates held therein."

The present application in another aspect relates to a wafer susceptor for retrofitting a single substrate deposition chamber, usually circular in shape, for processing of multiple wafer

substrates, so as to improve the overall wafer processing throughput (see the instant specification, page 6, lines 6-10).

Therefore, **such wafer susceptor is substantially circular in shape**, for fitting into a single substrate deposition chamber, **and comprises two or more recesses**, for holding two or more substrates to be processed in such single substrate deposition chamber, as illustrated in Figures 1B and 1C of the instant specification, and as expressly recited by new claim 51.

The wafer susceptor 90 of the Suda reference, although comprising two recesses 92 and 94, is not circular in shape (see Figures 5-7 and 12-14 of Suda) and is not designed for placement into and retrofitting a single substrate deposition chamber, as required by claims 51 and 52. Instead, such wafer susceptor 90 disclosed by Suda is a conventional batch wafer susceptor used in conjunction with a multiple substrate processing chamber 56 that is originally designed for processing multiple wafer substrates and is substantially oval in shape. Therefore, such wafer susceptor 90 also has an oval shape, for fitting into the oval multiple substrate processing chamber 56 (see Figures 5-7 and 12-14 of Suda).

Therefore, **Suda fails to teach or suggest in any manner a wafer susceptor for placement in a single substrate deposition chamber, which is substantially circular in shape and comprises two or more recesses**, as expressly required by new claims 51-52.

Such new claims 51 and 52 therefore patentably distinguish over Suda.

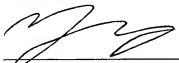
Conclusion

Claims 1-52 as amended/added herein are fully patentably distinguished over the cited reference, and in form and condition for allowance. Issue of a Notice of Allowance for the application is therefore requested.

A check payable to the Commissioner for Patents in the amount of $120 is enclosed herewith for payment of the fee for adding new claims 51 and 52. Please charge any deficiency and credit any excess payment to Deposit Account No. 08-3284 of Intellectual Property/Technology Law.

If any issues remain outstanding, incident to the formal allowance of the application, the Examiner is requested to contact the undersigned attorney at (919) 419-9350 to discuss same, in order that this application may be allowed and passed to issue at an early date.

Respectfully submitted,



Yongzhi Yang
Reg. No. (see attached)
Attorney for Applicant(s)

Steven J. Hultquist
Reg. No. 28,021
Attorney for Applicant(s)

INTELLECTUAL PROPERTY/ TECHNOLOGY LAW
P.O. Box 14329
Research Triangle Park, NC 27709
Phone: (919) 419-9350
Fax: (919) 419-9354
Attorney File No.: 2771-534 CIP

APPENDIX A

Clean Copy of All Pending Claims

1. A wafer susceptor for use in a substrate processing system, comprising:

at least one recess formed therein, wherein each recess is arranged and configured to hold one substrate therein, wherein said at least one substrate comprises material selected from the group consisting of silicon, gallium nitride, and aluminum nitride, and wherein said water susceptor is characterized by physical properties that match those of the substrates held therein.

2. The wafer susceptor of Claim 1, wherein said at least one substrate comprises silicon.

3. The wafer susceptor of Claim 1, wherein said physical properties comprise:

Thermal coefficient of expansion;

Reflectivity;

Thermal mass;

Thermal conductivity;

Electrical resistivity;

Dielectric constant;

Dielectric loss;

Density;

Hardness; and

Emissivity.

4. A substrate processing system comprising at least one wafer susceptor as in claim 1, wherein said system further comprises an automated substrate transport assembly arranged for transporting substrates into and out of a deposition chamber in which said wafer susceptor is disposed.

5. The substrate processing system of claim 4, wherein said automated substrate transport assembly is arranged for serially transporting single ones of a plurality of substrates into and out of said deposition chamber.

6. The substrate processing system of claim 4, further comprising a substrate cassette for storage and bulk transport of plural arrays of substrates, and said substrate cassette is positioned in substrate pickup and substrate delivery relationship to the automated substrate transport assembly.

7. The substrate processing system of claim 6, wherein said automated substrate transport assembly comprises a wand array comprising a plurality of wands constructed and arranged to simultaneously transport a corresponding plurality of substrates into and out of the deposition chamber, wherein the automated substrate transport assembly and the substrate cassette are constructed and arranged so that when the automated substrate transport assembly is translated into a pickup position relative to the substrate cassette, said plurality of wands engage and extract a plurality of substrates from the substrate cassette, with each wand engaging and extracting a substrate from a different one of said

plural arrays of substrates, and so that when the automated substrate transport assembly is translated into a deposit position relative to the substrate cassette, said plurality of wands release and deposit a plurality of substrates on the substrate cassette, with each wand releasing and depositing a substrate into a different one of said plural arrays of substrates.

8. The substrate processing system of claim 4, wherein said automated substrate transport assembly comprises a double-sided wand array comprising a plurality of wands constructed and arranged to simultaneously transport a corresponding plurality of substrates into and out of the deposition chamber.

9. The substrate processing system of claim 4, further comprising a loadlock chamber including a multiparted substrate cassette therein, and a transport arm arranged to selectively engage said multiparted substrate cassette and disengage from said multiparted substrate cassette in the loadlock chamber.

10. A substrate processing system comprising at least two wafer holders as in claim 1, an etch chamber for regeneration of wafer holders, and an automated transport assembly arranged to (1) introduce one of said at least two wafer holders into a deposition chamber, while another of said at least two wafer holders is disposed in said etch chamber and regenerated thereby, and (2) thereafter extract said at least two wafer holders respectively from the deposition chamber and etch chamber, followed by introduction of one of said at least two wafer holders into the etch chamber from the deposition chamber, and introduction of another of said at least two wafer holders into the deposition chamber from the etch chamber.

11. The substrate processing system of claim 10, wherein at least one of the wafer holders

has two recesses therein.

12. The substrate processing system of claim 10, wherein at least one of the wafer holders has four recesses therein.

13. The substrate processing system of claim 10, wherein at least one of the wafer holders a diameter in the range of from about 200mm to about 350mm.

14. The substrate processing system of claim 10, wherein at least one of the wafer holders has a diameter in the range of from about 200mm to about 300mm.

15. The substrate processing system of claim 10, wherein each of the wafer holders comprises recesses having a diameter in the range of from about 100mm to about 150mm.

16. The substrate processing system of claim 10, wherein each of the wafer holders comprises recesses having a diameter in the range of from about 100mm to about 125mm.

17. The substrate processing system of claim 10, further comprising a substrate cassette including slot members for positioning substrates in plural arrays, and wherein successive arrays are in side-by-side relationship to one another.

18. The substrate processing system of claim 17, wherein the substrate cassette is constructed and arranged for holding two arrays of substrates, wherein all substrates are planar and each respective substrate in a first array is generally coplanar with a corresponding

respective substrate in a second array.

19. The substrate processing system of claim 18, wherein the first and second arrays are parallel to one another.

20. The substrate processing system of claim 10, further comprising an automated substrate transport assembly and a substrate cassette, wherein the wafer holders, the automated substrate transport assembly, and the substrate cassette are constructed and arranged to simultaneously process two substrates.

21. The substrate processing system of claim 10, comprising a single wafer deposition chamber sized for processing single substrates having a 200mm diameter.

22. The substrate processing system of claim 21, wherein each wafer holder is arranged and configured for placement inside said single wafer deposition chamber, and each wafer holder comprises a plurality of recesses for holding substrates having a 100mm diameter.

23. The substrate processing system of claim 22, wherein each of the recesses in each wafer holder is circular.

24. The substrate processing system of claim 20, further comprising a processor for programmable operating the automated substrate transport assembly according to a cycle time program.

25. A method for increasing the throughput of a single substrate deposition chamber, said method comprising:

positioning in said single substrate deposition chamber a wafer susceptor having at least one recess formed therein, with each recess being arranged and configured to hold one substrate therein, wherein said at least one substrate comprises material selected from the group consisting of silicon, gallium nitride, and aluminum nitride, and wherein said water susceptor is characterized by physical properties that match those of the at least one substrate held therein.

26. The method of Claim 25, wherein said at least one substrate comprises silicon.

27. The method of Claim 25, wherein said physical properties comprise:

thermal coefficient of expansion;

reflectivity;

thermal mass;

thermal conductivity;

electrical resistivity;

dielectric constant;

dielectric loss;

density;

hardness; and

emissivity.

28. The method of claim 25, further comprising providing an automated substrate transport assembly including a wand array comprising a plurality of wands constructed and arranged to simultaneously transport a corresponding plurality of substrates into and out of the single substrate deposition chamber.

29. The method of claim 25, further comprising providing an automated substrate transport assembly arranged for serially transporting single ones of a plurality of substrates into and out of said single substrate deposition chamber.

30. The method of claim 25, further comprising providing an automated substrate transport assembly for transporting substrates into and out of said single substrate deposition chamber.

31. The method of claim 30, further comprising providing a substrate cassette for storage and bulk transport of plural arrays of substrates, wherein the cassette is positionable in substrate pickup and substrate delivery relationship to the automated substrate transport assembly.

32. The method of claim 31, wherein said automated substrate transport assembly comprises a wand array comprising a plurality of wands constructed and arranged to simultaneously transport a corresponding plurality of substrates into and out of the single substrate deposition chamber,

wherein said automated substrate transport assembly is first translated into a pickup position relative to the substrate cassette, so that the plurality of wands of said automated substrate transport assembly engage and extract a plurality of substrates from the

substrate cassette, with each wand engaging and extracting a substrate from a different one of the plural arrays of substrates in said substrate cassette;

wherein said automated substrate transport assembly subsequently carries the engaged and extracted substrates to the single substrate deposition chamber and releases the substrates into respective recesses in the wafer holder;

after deposition of thin film material on the substrates in the single substrate deposition chamber, yielding coated substrates, the automated substrate transport assembly extracts the coated substrates from the respective recesses in the wafer susceptor,

carries the extracted coated substrates, and releases the coated substrates to said substrate cassette or a second substrate cassette.

33. The method of claim 25, comprising using a double-sided wand assembly comprising a plurality of wands and arranged to simultaneously transport a corresponding plurality of substrates into and out of the single substrate deposition chamber.

34. The method of claim 25, comprising sequentially using multiple wafer holders, by positioning one of the multiple wafer holders in the single substrate deposition chamber for processing of wafers thereon, and concurrently regenerating another of said multiple wafer holders after it has been in the single substrate deposition chamber during processing of wafers thereon.

35. The method of claim 34, wherein said regenerating comprises etch processing of said another of said wafer holders.

36. The method of claim 25, wherein the wafer holder has two recesses therein.

37. The method of claim 25, wherein the wafer holder has four recesses therein.

38. The method of claim 25, wherein the wafer holder has a diameter in the range of from about 200 mm to about 350 mm.

39. The method of claim 25, wherein the wafer holder has a diameter in the range of from about 200 mm to about 300mm.

40. The method of claim 38, wherein each of the recesses in said wafer holder has a diameter in the range of from about 100mm to about 150mm.

41. The method of claim 38, wherein each of the recesses in said wafer holder has a diameter in the range of from about 100mm to about 125mm.

42. The method of claim 25, further comprising providing a substrate cassette including slot members for positioning substrates in plural arrays, and wherein successive arrays are in side-by-side relationship to one another.

43. The method of claim 25, further comprising providing a substrate cassette that is constructed and arranged for holding two arrays of substrates, wherein all substrates are planar and each respective substrate in a first array is generally coplanar with a corresponding respective substrate in a second array.

44. The method of claim 43, wherein the first and second arrays are parallel to one another.

45. The method of claim 25, further comprising providing an automated substrate transport assembly and a substrate cassette, wherein the single substrate deposition chamber, the automated substrate transport assembly, and the substrate cassette are constructed and arranged to simultaneously process two substrates.

46. The method of claim 25, wherein the single wafer deposition chamber is sized for processing single substrates having a 200mm diameter.

47. The method of claim 46, wherein the wafer holder comprises a plurality of recesses arranged and configured to hold substrates having a 100mm diameter.

48. The method of claim 47, wherein each of the recesses is circular.

49. The method of claim 25, further comprising providing an automated substrate transport assembly for transporting substrates into and out of the single substrate deposition chamber, and programmably operating the automated substrate transport assembly according to a cycle time program.

50. A wafer susceptor used in a semiconductor substrate processing system, comprising at least one recess formed therein, wherein each recess is arranged and configured to hold one semiconductor substrate therein, wherein said at least one semiconductor substrate comprises material selected from the group consisting of silicon, gallium nitride, aluminum nitride, diamond, gallium arsenide, indium nitride, indium phosphide, and gallium phosphide, wherein said wafer susceptor is characterized by physical properties that match those of the semiconductor substrates held therein.

51. A wafer susceptor arranged and configured for placement in a single substrate deposition chamber, wherein said wafer susceptor is substantially circular in shape and comprises two or more recesses formed therein, wherein each recess is arranged and configured to hold one substrate, and wherein said water susceptor is characterized by physical properties that match those of the substrates held therein.

52. The wafer susceptor of claim 51, wherein the substrates comprise material selected from the group consisting of silicon, GaN, SiC, and AlN.

BEFORE THE OFFICE OF ENROLLMENT AND DISCIPLINE
UNITED STATE PATENT AND TRADEMARK OFFICE

LIMITED RECOGNITION UNDER 37 CFR § 10.9(b)

Yongzhi Yang is hereby given limited recognition under 37 CFR § 10.9(b) as an employee of Steven J. Hultquist to prepare and prosecute patent applications wherein the patent applicant is the client of Steven J. Hultquist, and the attorney or agent of record in the applications is a registered practitioner who is a member of the Intellectual Property/Technology Law firm. This limited recognition shall expire on the date appearing below, or when whichever of the following events first occurs prior to the date appearing below: (i) Yongzhi Yang ceases to lawfully reside in the United States, (ii) Yongzhi Yang's employment with Steven J. Hultquist ceases or is terminated, or (iii) Yongzhi Yang ceases to remain or reside in the United States on an H-1 visa.

This document constitutes proof of such recognition. The original of this document is on file in the Office of Enrollment and Discipline of the U.S. Patent and Trademark Office.

Expires: August 1, 2003

Harry I. Moatz
Director of Enrollment and Discipline